

REMARKS

Claims 1, 3-5, 13, 15-17, 25, and 27-29, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 3-5, 13, 15-17, 25, and 27-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ma, et al. (U.S. Patent No. 6,509,622), hereinafter referred to as Ma, in view of Kishida, et al. (U.S. Publication No. 2001/0053948), hereinafter referred to as Kishida. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a methodology for displaying a guard ring within an integrated circuit design, comprising displaying a parameterized symbol and displaying parameters. In the rejection, the Office Action argues that Ma discloses logic devices and guard rings that symbolically comprise a parameterized symbol. However, Ma does not disclose a method of displaying a guard ring, comprising displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action asserts that Ma teaches logic devices and guard rings that symbolically comprise a parameterized symbol. More specifically, the Office Action

argues that Ma discloses a type of circuit or device logic, such as analog, digital, and mixed signal circuit (citing col. 2, ll. 20-29), and a type of guard ring associated with area of electronic devices (citing col. 2, ll. 55-60). Further, the Office Action argues that Ma discloses guard ring efficiency, such as width, thickness, depth and the electrical characteristics (citing col. 3, ll. 46-67, col. 4, and col. 5, ll. 1-32).

However, nothing in Ma discloses displaying such parameters. In addition, nothing in Ma teaches or suggests displaying a parameterized symbol or displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring. These features are defined in independent claims 1, 13 and 25 using the following language: "displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring."

In column 6, lines 14-18, Ma discloses a display 503 coupled to a microprocessor. As illustrated in FIG. 5, the display 503 is any display capable of being coupled to a microprocessor. While display 503, in one embodiment, may be a cathode ray tube display, in other embodiments, display 503 may be a liquid crystal display. However, unlike the claimed invention, the display 503 does not display a parameterized symbol. Further unlike the claimed invention, the display 503 does not display parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring. Ma merely states that the computerized device 501 (which comprises guard rings 105 and the display 503) is suitable for use in connection with the present invention.

Therefore, contrary to the position taken in the Office Action, Applicants submit that Ma does not teach or suggest a method of displaying a guard ring within a hierarchical integrated circuit design comprising displaying a parameterized symbol and displaying parameters. Thus, it is Applicants' position that Ma does not disclose or suggest the claimed feature of "displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring" as defined by independent claims 1, 13 and 25.

Accordingly, Applicants respectfully submit that it would not have been obvious to combine Ma with Kishida to arrive at the claimed invention. It is Applicants' position that the proposed combination of Ma and Kishida do not teach or suggest many features defined by independent claims 1, 13 and 25 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 3-5, 15-17, and 27-29 are similarly patentable, not only because of their dependency from patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1, 3-5, 13, 15-17, 25, and 27-29, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 1/3/06



Duane N. Moore, Esq.
Registration No. 53,352

Gibb I.P. Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
(410) 573-6501
Customer Number: 29154